

Greyscale in Zenithal Bistable LCD: The Route to Ultra-low Power Colour Displays.

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ABSTRACT

Zenithal Bistable Devices (ZBD™) exhibit rugged image storage, excellent optical performance, fast latching and infinite multiplexibility. These properties arise from the use of the grating layer used to align a nematic liquid crystal. Such gratings also offer a high degree of design flexibility. In the present work, grating shape is varied within each pixel to introduce error-free analogue greyscales. Passive matrix waveforms, suitable for use with commercial STN drivers are reported, and shown to produce at least 7 error-free greys in a test cell. A method for achieving 64 static greys is described.

Keywords: LCD, bistability, greyscale, colour, ZBD.

INTRODUCTION

An essential part of producing colour displays is the achievement of sufficient greyscale. For example, 4096 colours require 16 separately addressable transmission (or reflection) levels. Bistable display technologies are inherently digital in nature. Full colour bistable ferroelectric liquid crystal displays have been reported: 256 greys were achieved using a combination of spatial (electrode subdivision) and temporal dither (frame subdivision) [1]. However, temporal dither requires fast operation and cannot be used in an image storage mode. A high level of spatial dither is costly, both in terms of the additional electronic drivers needed, and the electrode etching limits for the least significant bit.

An analogue approach to generate the grey levels is often taken for devices such as the bistable cholesteric, in which partial latching of the pixel is used [2]. After blanking into one of the stable states, an intermediate voltage level nucleates domains of the opposite state, forming a random mixture of domains. Such an approach is sensitive to panel variations because the latching threshold is dependent on the applied voltage, cell gap and temperature. Any variation of condition across the panel will cause some change in the transmission or reflection from the pixel. To prevent overlapping grey levels, these tolerances can become very tight. For example, considering cell gap variations alone, sixteen analogue levels require cholesteric devices to be produced with tolerances of ± 11 nm [3]. Bistable Twisted Nematic devices rely on obtaining the correct ratio of cell gap and helical pitch, and need tighter tolerances still to obtain reliable greyscale.

Zenithal Bistable Devices [4] use a grating alignment layer to give two stable states of a nematic liquid crystal, either high or low surface tilt. When used opposite

a conventional rubbed alignment surface, the device may be latched between HAN and TN configurations (Figure 1) using bipolar pulses of sufficient energy. Displays have been produced that show excellent front-of-screen performance, combined with ultra-low power and rugged image storage [5]. This is achieved using a standard $5\mu\text{m}$ cell gap, and with manufacturing tolerances closer to those of conventional TN displays, rather than STN.

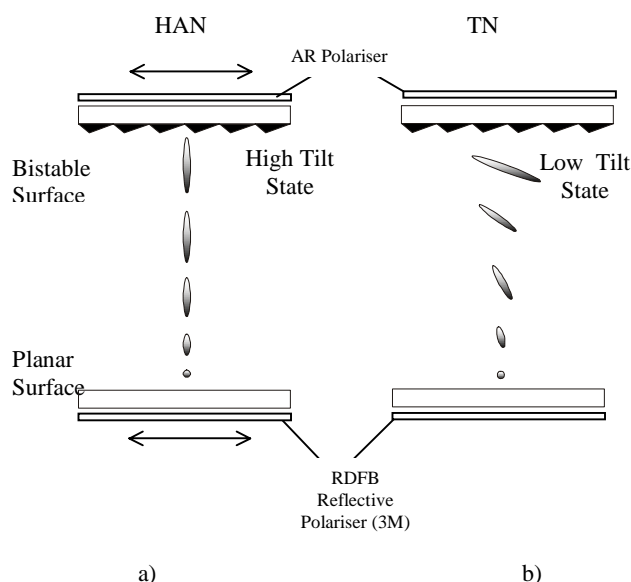


Figure 1. Schematic of the ZBD cell configuration: a) high tilt (HAN) and b) low tilt (TN) alignment states.

ERROR-FREE GREYSCALE

An important advantage of grating alignment layers is the design flexibility that they offer. The shape and alignment properties of the grating may be varied across a pixel, for example to give wide viewing angle and analogue greyscales [6]. For example, each pixel can be subdivided into a number of areas with different latching thresholds; the fraction of the pixel that changes state, and hence its transmission, is then related to the applied electrical signal. Alternatively, appropriate grating design [7], introduces further stable pre-tilts of the director and hence gives a zenithal multistable device. Both of these approaches lead to error-free greys, as shown by curve B in Figure 2. Within the limits set by the partial latching regions of adjacent thresholds, the transmission of error-free greys is independent of cell variations.

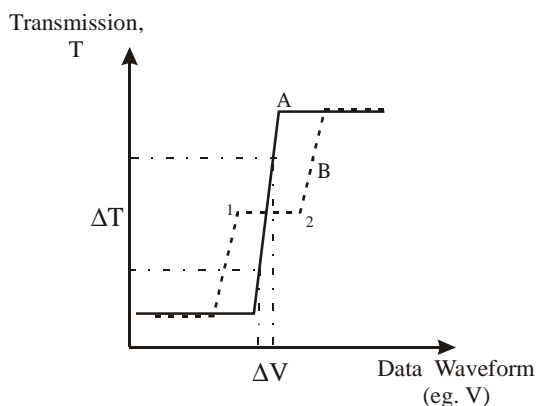


Figure 2. The principle of error-free grey levels. Curve A represents a typical latching response of a domain nucleated bistable device. Slight variations in the conditions across a cell (such as ΔV) lead to relatively large transmission errors (ΔT). Curve B shows the response to a similar device with an intermediate threshold level and the same partial latching width. Between voltages 1 and 2, the transmission is independent of ΔV and the grey level is error-free.

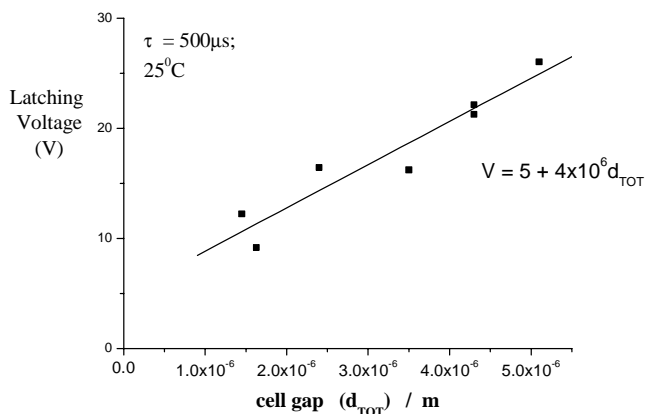
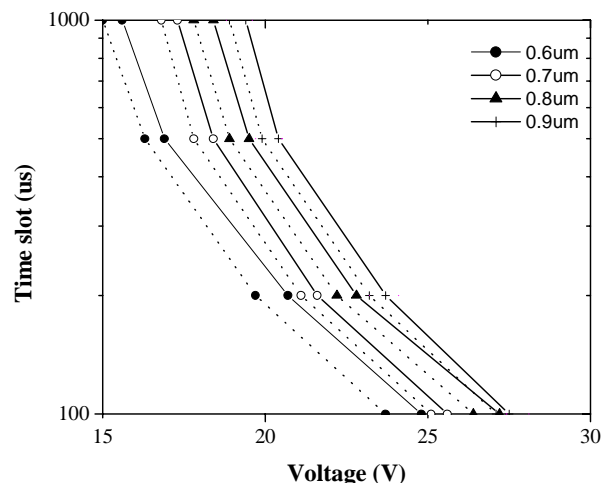


Figure 3. Cell gap dependence of the ZBD latching voltage (for a 500 μ s bipolar pulse at 25 $^{\circ}$ C).

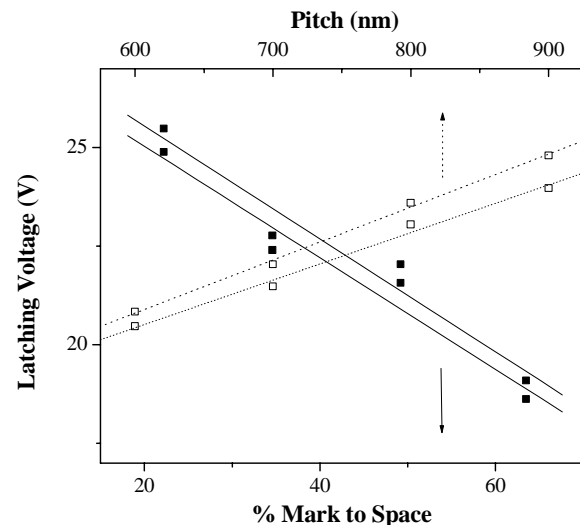
A typical ZBD cell gap dependence is shown in Figure 3. Latching is a field effect (requiring 4V/ μ m for this material) and the offset is due to the dielectric effect of the grating layer. Conventional TN requires a cell gap tolerance of $\pm 0.2\mu$ m (to prevent optical variations), whereas STN requires lower tolerances, typically $\pm 0.05\mu$ m. Such cell gap deviations across a ZBD panel would change the latching threshold by 0.8 V and 0.2 V, respectively. Note, the cell gap tolerance for optical variations is the same for ZBD as TN.

There are several practical options for varying the latching threshold of the grating, including changes of pitch, amplitude, mark to space ratio and offset. Test cells were fabricated using sub-pixels with pitches in the range 0.6 μ m to 1.0 μ m, and mark to space ratios from 22% to 64%, whilst keeping amplitude and offset fixed. The latching threshold characteristics for these cells are shown in Figure 4. Excellent bistability was maintained across this range of grating shapes: the latching energy reduced approximately linearly with decreasing pitch, and increased with decreasing mark to space ratio. The ZBD latching

threshold changed by 6 V across the window of bistability, and the partial latching width is typically 0.4 V. This means that 6 error-free analogue levels may be achieved in ZBD panels made to TN tolerances, whereas 15 error-free levels are possible if STN tolerances are maintained. Other changes to the grating shape, such as change in offset, will increase the tolerance to variations and allow further error-free greys to be produced.



a)



b)

Figure 4. ZBD latching characteristic as a function of grating shape. a) τV curves for a range of grating pitch. b) Latching voltage dependences on pitch and mark to space ratio. The lower line represents onset of domain nucleation, and the upper line complete latching.

GREYSCALE ADDRESSING USING COMMERCIAL STN DRIVERS

Although commercially preferable, the use of STN drivers constrains the addressing schemes that can be used to drive a bistable display. For example, the drivers are usually restricted to five voltage levels (e.g. 0, $\pm V_s$ and $\pm V_d$), wherein the data voltage, $V_d \leq 7$ V but cannot include periods of 0 V. This means that amplitude modulated data waveforms are unsuitable for selecting the required grey level. Moreover, the waveforms should be DC balanced

within each line address time because ZBD response to the polarity of the applied signal.

The approach taken in the present work was to use either four or six time slots for each addressed line. A bipolar strobe signal of either $(++/-)Vs$ or $(+++/---)Vs$ was applied to the addressed row synchronously with the appropriate data waveform on the columns. All other rows were set at 0 V. With the four slot schemes, there are 6 permutations of data waveform: $(++/-)Vd$, $(+/-+)Vd$, $(+/-+)Vd$, $(-+/+)Vd$, $(-+/+)Vd$ and $(-/++)Vd$. With the six slot schemes, there are 20 data waveform permutations, as listed in Table 1.

Table 1. Example data waveforms for a six slot scheme suitable for addressing analogue levels when combined with the bipolar strobe $(+++/---)Vs$.

Number	Data waveform (.../...)Vd	Maximum Voltage swing (V)	Trailing pulse energy factor
1	+++/---	$2(Vs-Vd)$	-3
2	-++/-+	$2(Vs-Vd)$	-1
3	-++/-+	$2(Vs-Vd)$	-1
4	+--/-++	$2(Vs-Vd)$	-1
5	+--/-++	$2(Vs-Vd)$	-1
6	--+/-++	$2(Vs-Vd)$	+1
7	++/-++	$2Vs$	-1
8	++/-++	$2Vs$	-1
9	-+/-++	$2Vs$	+1
10	-+/-++	$2Vs$	+1
11	-++/+--	$2Vs$	-1
12	-++/+--	$2Vs$	-1
13	--+/++	$2Vs$	+1
14	--+/++	$2Vs$	+1
15	++/+--	$2(Vs+Vd)$	-1
16	-+/-++	$2(Vs+Vd)$	+1
17	+--/+--	$2(Vs+Vd)$	+1
18	-+/-++	$2(Vs+Vd)$	+1
19	+--/+--	$2(Vs+Vd)$	+1
20	---/+++	$2(Vs+Vd)$	+3

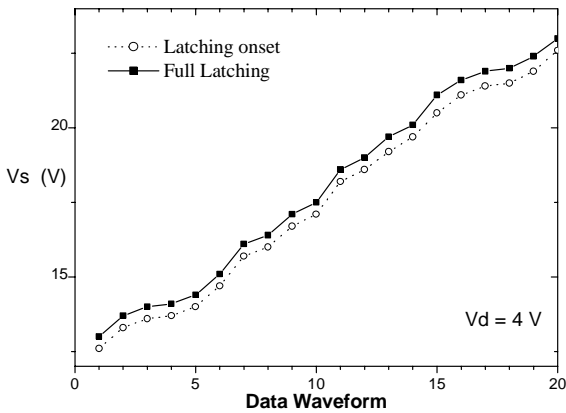


Figure 5. Latching Voltage as a function of data waveform for the six-slot scheme of Table 1.

To help ensure each of the required greys is achieved, the operating window for each must be as wide as

possible. This occurs when the latching energy (e.g. Vs) is a linear function of the applied waveform. Figure 5 shows typical results for the six-slot scheme. The limited number of permutations of the four-slot scheme did not give sufficient flexibility to ensure linearity of the greyscale response. Two aspects of the resultant waveform shape effect the latching: the select (trailing) pulse energy and the maximum voltage swing. The swing has the larger effect on latching voltage, but the smaller effect of trailing pulse energy allows fine-tuning to ensure the linearity.

Figure 6 illustrates the optical response for 5 transitions induced in a pixel sub-divided into 8 areas of different grating shapes by changing the pulse amplitude. Figure 7 includes photomicrographs of this device addressed using the multiplexing waveforms of table 1. This clearly illustrates that at least 6 separately addressable areas may be discriminated using waveforms readily produced using conventional STN drivers. The lack of partial latching in each case is indicative of the error-free nature of these transmission levels. Of course, it is also possible to achieve many more greys by partially latching each of the sub-divisions. Such levels, however, will not be error-free, and will change with panel variations in a similar fashion to that of a cholesteric device.

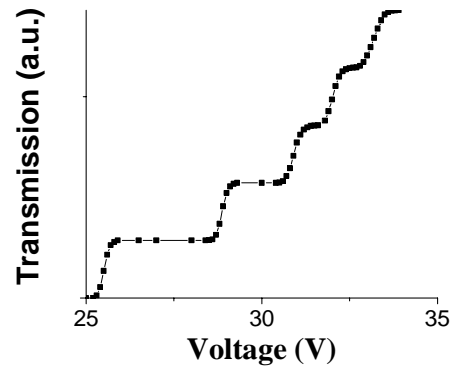


Figure 6. Pixel transmission versus addressing pulse amplitude. ($\tau = 50\mu s$, $T = 25^\circ C$)

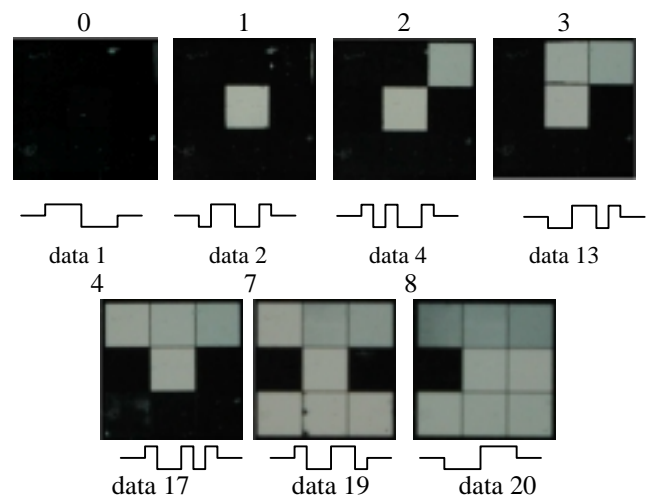


Figure 7. Photo-micrographs of a pixel divided into 8 latchable areas (of which 6 are non-degenerate), together with the data waveforms used to generate the patterns. ($\tau=30\mu s$, $Vs=24V$, $Vd=4V$).

ACHIEVING HIGH NUMBERS OF GREYSCALE

Significantly more greys can be achieved using only two bits of spatial dither. Linearly spaced levels without redundancy are possible using an appropriate weighting factor for each of the digital bits. With n analogue levels, the sub-pixels should be weighted $1 : n : n^2 \dots n^{(a-1)}$, thereby giving a total of n^a levels [8]. For example, 16 levels are possible with 2 bits of spatial dither ($a=2$) and four analogue levels by weighting the sub-pixels in areas of 1 : 4, as shown in figure 8. For a 210 μm square pixel, this requires a 38 μm wide least significant bit, and three grating areas of 67 μm width (assuming a 10 μm inter-pixel gap). Although 64 levels are possible from only 8 analogue levels, the narrow width of the least significant bit required (21 μm for the example of figure 8) may be impractical to fabricate and address. In this instance, it may be preferable to use a lower spatial dither weighting and thereby introduce redundant greys, as shown in Figure 9. For example, the combination of 8 analogue levels and 1:4 spatial dither gives 36 separate grey levels. Moreover, offsetting the digital weighting slightly reduces the degree of redundancy.

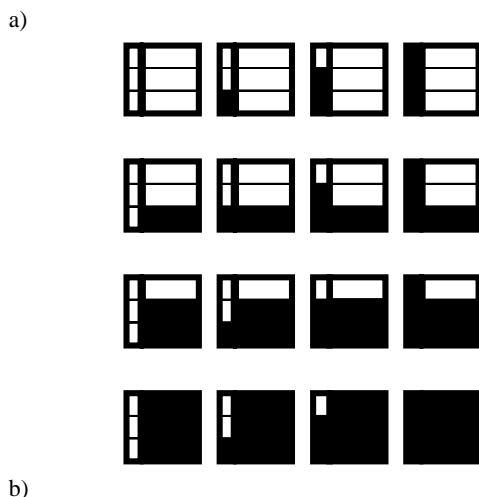
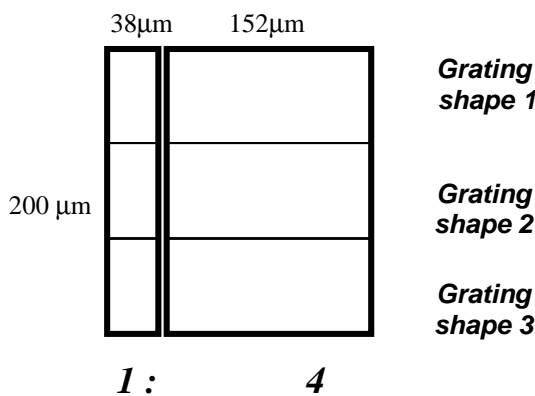


Figure 8. Optimum pixel design for achieving 16 error-free grey levels, by combining four analogue levels with 2 bits of spatial dither.

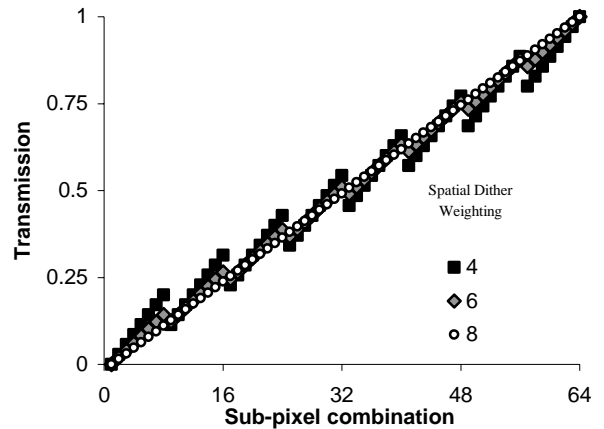


Figure 9. Effect of different sub-pixel weighting factors on the greyscale characteristic.

CONCLUSION

Error-free grey levels are easily introduced in ZBD devices without extra cost to the panel, as STN drivers may still be used and the extra-complexity is put into the grating production. Much higher levels of greyscales are possible when error containing greys are also used, and in combination with spatial dither. In the future, we will describe methods [9] by which the extra electrodes used in spatial dither can be driven without increasing driver requirements.

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